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# An E-Band Low-Noise Transformer-Coupled Quadrature VCO in 40 nm CMOS

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**Abstract**— This paper presents a Transformer-Coupled Quadrature VCO (TC-QVCO) designed to achieve low-noise performance at millimeter-wave. The VCO core is implemented combining the tuned-input tuned-output (TITO) oscillator and the Colpitts oscillator, while the coupling is realized by means of transformers, resulting in low noise and accurate quadrature phases. Designed in a 40 nm CMOS process, the TC-QVCO operates between 83.7 GHz and 88.7 GHz (i.e., 5.8% tuning range). Dissipating 28.4 mW from a 0.7 V supply, the measured phase noise is -118.8 dBc/Hz at 10 MHz offset from a 88.7 GHz carrier, resulting in a peak phase-noise FoM of -183.2 dBc/Hz. The I/Q phase error is less than 1.2° over the whole tuning range

**Keywords**— *quadrature voltage-controlled oscillator (VCO), millimeter-wave oscillators, low phase noise, CMOS*

## 1 Introduction

The increasing demand for high data rate low cost communication links pushes companies and research institutes toward wireless solution at higher frequencies. To satisfy this request, both FCC in USA and CEPT in Europe have recently allocated two channels of 5 GHz each in the E-Band (i.e., 71-76 GHz and 81-86 GHz), thus making long distance high data rate wireless point-to-point communications possible. To achieve high spectral efficiency, complex digital modulation schemes should be adopted. However, such techniques impose severe requirements on the frequency synthesizer, in particular in terms of phase noise. Moreover, the higher the frequency, the higher the impact of parasitic, making the tradeoff between tuning range, phase noise and power consumption tighter.

This paper describes a CMOS frequency generation circuit with quadrature outputs capable of withstanding the impact of the aforementioned parasitics while providing low phase noise over the 5 GHz band between 81 and 86 GHz. In this scenario, two fundamental VCOs and a way of coupling are needed. The former can be implemented combining the tuned-input tuned-output (TITO) oscillator and the Colpitts oscillator (as presented in [1]), while the latter can be achieved by means of gate to drain transformer coupling (similarly to the work presented in [2]).

This paper is organized as follow. Section II describes the proposed Transformer-Coupled Quadrature VCO. Section III presents the circuit design and implementation. Section IV summarizes the measurement results. Finally, conclusions are drawn in Section V.

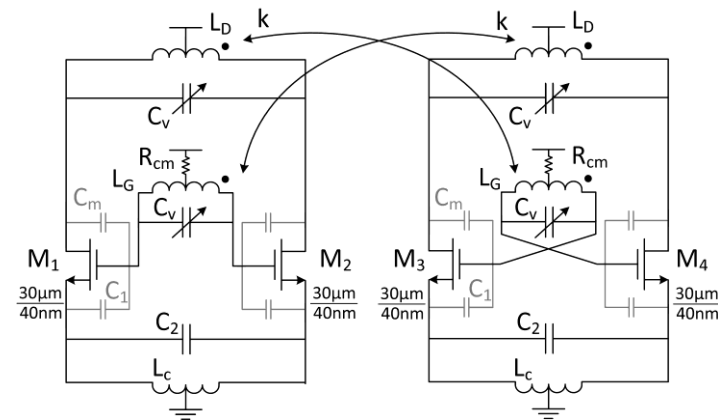


Fig. 1. Schematic view of the proposed Transformer-Coupled Quadrature VCO (TC-QVCO).

## 1 Proposed Transformer-Coupled Quadrature VCO

A fundamental QVCO is composed by two elements, 1) two identical VCOs and 2) a mean of coupling. Intuitively, to achieve the best phase noise performance, a low noise oscillation core should be adopted together with a coupling mechanism that degrades performance as little as possible. Reference [1] proposes a fundamental VCO implemented combining the TITO oscillator and the Colpitts one. This technique proves adequate to tolerate extensive parasitics, resulting in excellent phase noise performance at mm-Wave. Regarding the coupling mechanism, a realization by means of passive devices (e.g., transformers) brings several advantages, especially at mm-Wave [2], [3]. As a matter of fact, the popular parallel-coupled QVCO proves sensitive to the flicker noise of the coupling active devices [4], and shows a critical trade-off between phase error and phase noise [5]. Furthermore, the values of the inductor needed to realize the tank decreases with frequency. Therefore, at the frequency of interest it is possible to implement transformers with no need of extensive silicon area and without loading the tank with large parasitic capacitance to the substrate.

Fig. 1 shows the proposed Transformer-Coupled Quadrature VCO (TC-QVCO), realized by adopting a combination of the TITO and Colpitts topology for the two oscillation cores and gate to drain transformers as mean of coupling.

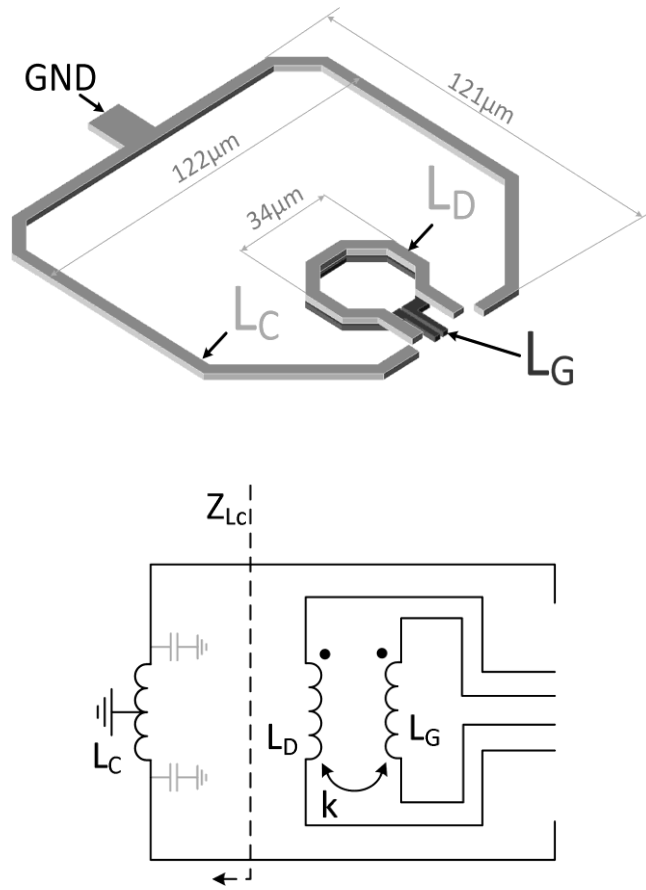


Fig. 2. 3-D view (top) and simplified lumped model (bottom) of transformer and choke inductor.

## 1.1 Circuit Analysis

To achieve the high oscillation frequency required,  $C_m$  and  $C_1$  depicted in Fig. 1 can be realized by means of the MOS parasitic capacitances  $C_{gd}$  and  $C_{gs}$  respectively.  $L_c$  behaves as a choke inductor, to provide the DC feed, while the value of  $C_2$  can be optimized for phase noise performance, in a fashion similar to the conventional Colpitts oscillator [6].

The resonant frequencies of the proposed TC-QVCO can be derived as follow:

$$\omega_0^2 \cong \frac{C_d + C_g + 2C_m \pm \sqrt{(C_d - C_g)^2 + 4C_m^2 + 4k^2[(C_d + C_g)C_m + C_d C_g]}}{2L_0(1 - k^2)[(C_d + C_g)C_m + C_d C_g]} \quad (1)$$

where  $C_g = 2C_v + C_1 2C_2 / (C_1 + 2C_2)$ ,  $C_d$  is the sum of  $2C_v$  and the parasitic capacitance from the drain node to ground, and  $L_0 = L_G / 2 \approx L_D / 2$ .

Equation (1) shows that this architecture can resonate at two different frequencies. However, when these two tones are spaced enough, only the lower one can meet the Barkhausen's criteria. In fact, at the higher frequency, the tank losses become larger and the active devices fail to provide enough negative transconductance to sustain the oscillation.

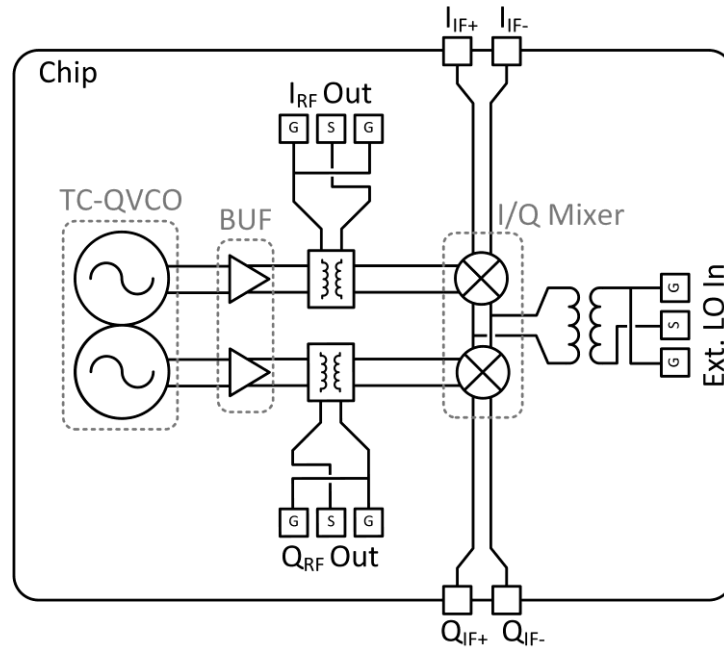


Fig. 3. Block diagram of the TC-QVCO test chip.

Furthermore, this structure can oscillate both in differential mode, and in common mode. To overcome this limitation,  $R_{cm}$  can be implemented on chip, providing the required bias voltage at the gate of  $M1/M2/M3/M4$  while degrading the quality factor of the tank only for the common mode oscillation.

## 1.2 Transformer and $L_c$ Design

Fig. 2 presents the layout and the simplified lumped element model of the transformer and the choke inductor  $L_c$ . The transformer is implemented by the two top metals M9 and M10, where the outer diameter of the octagonal windings is  $34\text{ }\mu\text{m}$ , with a width of  $4\text{ }\mu\text{m}$ . To accurately model all layout-dependent parasitics of the interconnecting metals as well as passive components, a 2.5D EM-simulator (i.e., ADS Momentum) is used. The primary and secondary self-inductances of the transformer are about  $L_D = 51\text{ pH}$  and  $L_G = 57\text{ pH}$ , with  $Q_D = 15$  and  $Q_G = 14$ . The self-resonant frequencies exceed  $200\text{ GHz}$ . The transformer coupling factor  $k$  is  $0.52$ . Noteworthy, since the voltage waveforms across the transformer are almost in-phase, the large interwinding capacitance of this structure can be neglected.

The proposed TC-QVCO topology in Fig. 1, needs a choke inductor  $L_c$  to provide the DC feed and a parallel capacitance  $C_2$ . To realize  $L_c$  on chip, a large third winding is drawn in M10 (see Fig. 2). Due to the considerable parasitic coupling to the substrate,  $L_c$  can not be model as an ideal inductor. Moreover, the effect of these parasitics proves to be beneficial. As a matter of fact, at the frequency of interest  $Z_{L_c}$  shows a capacitive behavior, and can be therefore modelled as a DC feed in parallel with a capacitance which can be incorporated in  $C_2$ .

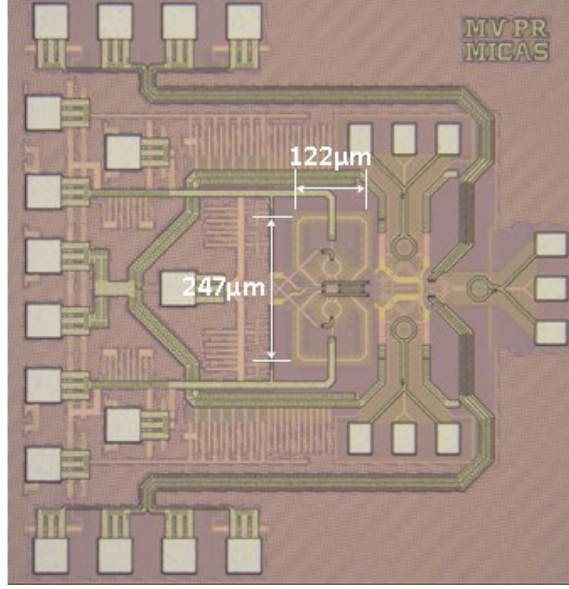


Fig.4. Die photograph of the Transformer-Coupled Quadrature VCO (247μm·122μm).

## 2 Circuit Design and Implementation

To ensure reliable start-up conditions the transconductors  $M1/M2/M3/M4$  have been sized up to an aspect ratio of 30μm/40nm. From post layout simulation, the parasitic capacitances of the MOS are estimated as  $C_{gd} = 8.5$  fF and  $C_{gs} = 18$  fF.  $C_2$  is implemented with the parasitic capacitance at the source node and a MOM capacitor of 12 fF. In this design the space between the two resonant frequencies derived in (1) is larger than 70 GHz across the tuning range, thus the VCO will sustain the oscillation only at the desired frequency. Furthermore, a value of  $R_{cm}$  larger than 100Ω ensures common mode stability.

For testing purpose, a buffer and a double-balanced mixer are also implemented on chip, as shown in Fig. 3. The buffer consists of a neutralized CS amplifier, showing high input-output isolation while providing the mm-Wave signal to the GSG probe pads and driving the mixer. The latter, instead, is based on a Gilbert cell. The supply voltage used for the oscillator core is 0.7 V, while the one used for the buffer and the mixer is set to the nominal voltage 0.9 V.

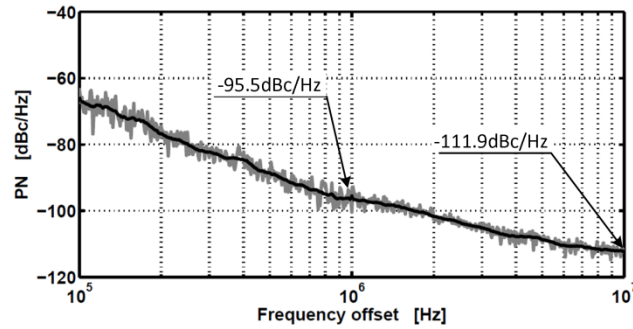


Fig. 5. Measured phase noise at 84.6 GHz.

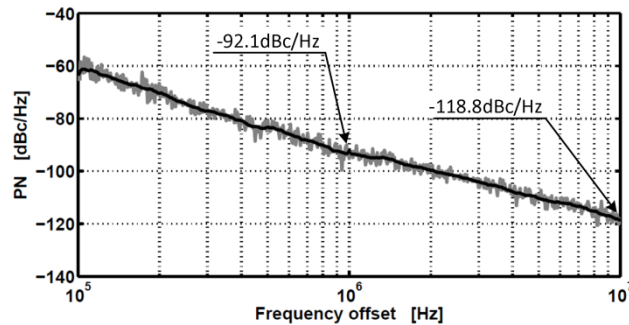


Fig. 6. Measured phase noise at 88.7 GHz.

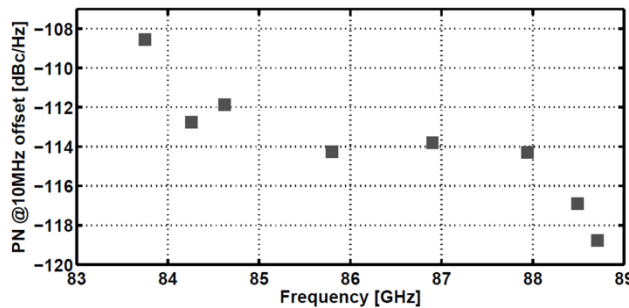


Fig. 7. Measured phase noise at 10 MHz offset across the tuning range.

### 3 Measurement Results

Fig. 4 shows the die photograph of the Transformer-Coupled Quadrature VCO, designed and fabricated in a 40 nm bulk CMOS process. The prototype occupies a core area of  $247\mu\text{m} \times 122\mu\text{m}$ . The TC-QVCO covers a tuning range of 5 GHz between 83.7 GHz to 88.7 GHz. The measured oscillation frequency is only 3.3% higher than expected.

To perform phase noise measurements, one of the mm-Wave output signals is downconverted with an external W-band harmonic mixer and applied to a PXA Agilent signal analyzer. Fig. 5 shows the measured phase noise at 84.6 GHz, namely -95.5 dBc/Hz and -111.9 dBc/Hz at 1 MHz and 10 MHz offset respectively. Fig. 6 shows the measured phase noise at 88.7 GHz, namely -92.1 dBc/Hz and -118.8 dBc/Hz at 1 MHz and 10 MHz offset respectively. Within the tuning range the phase noise varies between -90.8 dBc/Hz and -95.5 dBc/Hz at 1 MHz offset. The phase noise at 10 MHz offset versus the oscillation frequency is shown in Fig. 7. The power dissipation is 28.4 mW from a 0.7 V supply. This yields a figure-of-merit (FoM) that ranges from -174.7 to -179.5 dBc/Hz at 1 MHz offset and from -172.5 to -183.2 dBc/Hz at 10 MHz offset across the tuning range.

To measure the I/Q imbalance, an external signal is applied to the double balanced quadrature on-chip mixer driven by the TC-QVCO (see Fig. 3). The downconverted quadrature signals are measured with an Agilent Infinium oscilloscope. Fig. 8 shows I/Q signals



downconverted to 550 MHz. The phase error and the amplitude error are less than 1.2° and 1dB respectively over the complete tuning range, proving the accurate quadrature generation of this architecture.

TABLE I. COMPARISON WITH STATE-OF-THE-ART MM-WAVE CMOS QVCOs

TABLE II. F.	RE	Freq. (GHz)	PN @1MHz (dBc/Hz)	FOM @1MHz (dBc/Hz)	PN @10MHz (dBc/Hz)	FOM @10MHz (dBc/Hz)	Phase error	Power (mW)	Tech.	Area (mm <sup>2</sup> )
ISSCC 2011 [2]		56.0-60.4 <sup>a</sup> (7.6%)	-95/-97 <sup>b</sup>	-176.9/-178.9 <sup>b</sup>	-117	-178.9	< 1.5°	22	65nm	0.075
ISSCC 2014 [3]		53.8-63.3 <sup>a</sup> (16.2%)	-92.5	-173.1	n.a.	n.a.	< 4.8°	30 <sup>c</sup>	40nm	0.075 <sup>d</sup>
ESSCIRC 2012 [7]		48.8-62.3 <sup>a</sup> (24.3%)	-90/-94 <sup>b</sup>	-173/-176 <sup>b</sup>	n.a.	n.a.	n.a.	15.6/30	65nm	0.112
RFIC 2013 [8]		120 (13.5%)	-87	-170.5	-112	-175.5	< 5°	64	45nm	0.2
ISSCC 2013 [9]		57.88-68.3 <sup>a</sup> (16.6%)	-94.2	-179.6	-115	-180.4	< 0.7°	11.4	65nm	0.039
ISSCC 2008 [10]		93.1 (4.3%)	-90	-172.7	n.a.	n.a.	n.a.	43.2	65nm	n.a.
<b>This Work</b>		<b>83.7-88.7<sup>a</sup></b> <b>(5.8%)</b>	<b>-90.8/-95.5<sup>b</sup></b>	<b>-174.7/-179.5<sup>b</sup></b>	<b>-108.5/-118.8<sup>b</sup></b>	<b>-172.5/-183.2<sup>b</sup></b>	<b>&lt; 1.2°</b>	<b>28.4</b>	<b>40nm</b>	<b>0.030</b>

<sup>a</sup>  $f_{\min}$ - $f_{\max}$

<sup>b</sup> Worst/best measured performance within the tuning range

<sup>c</sup> QVCO core + buffer

<sup>d</sup> Graphically estimated

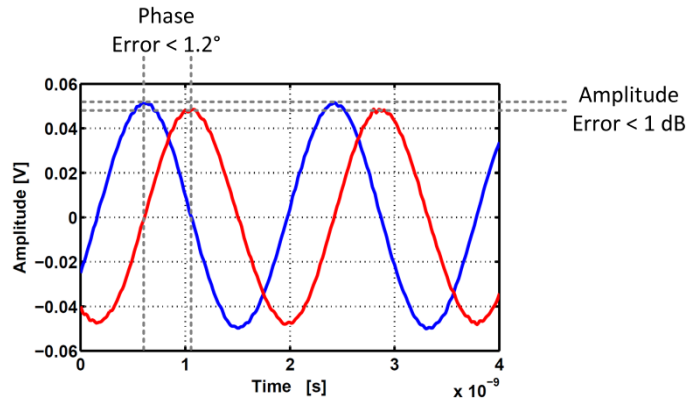


Fig.8. Measured phase and amplitude imbalance of the I/Q signals downconverted to 550 MHz.

Table I summarizes the comparison with the state-of-the-art mm-Wave CMOS QVCOs. Thanks to the proposed circuit techniques, this work achieves low noise performance within the 5 GHz required band, while providing low I/Q imbalance and consuming a small silicon area. To the best of the authors' knowledge, this is the first E-Band QVCO implemented in 40 nm CMOS technology.

## 4 Conclusion

We have proposed an E-Band Transformer-Coupled Quadrature VCO (TC-QVCO) implemented by two fundamental oscillators coupled by gate to drain transformers. The core





VCO combines the TITO and the Colpitts topology, providing low noise performance at mm-Wave. As a result, the prototype realized in 40 nm CMOS technology shows a state-of-the-art phase noise of -118.8 dBc/Hz at a 10 MHz offset from a 88.7 GHz carrier, resulting in a phase-noise FoM of -183.2 dBc/Hz, while providing accurate quadrature phases.

## 5 Acknowledgment

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